




# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,058	10/04/2004	John Barrett George	PU020090	4273
24498	7590	09/07/2005	EXAMINER	
THOMSON LICENSING INC. PATENT OPERATIONS PO BOX 5312 PRINCETON, NJ 08543-5312			KITOV, ZEEV	
			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/510,058	GEORGE ET AL. 	
	<b>Examiner</b>	<b>Art Unit</b>	
	Zeev Kitov	2836	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1 - 6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 October 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/04/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "a power supply output transistor for generating a first power supply current of a load circuit and a second power supply current of said first amplifier stage" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

The Specification is objected to due to a following reason. The following subject matter claimed in Claim 1: "a power supply output transistor for generating a first power supply current of a load circuit and a second power supply current of said first amplifier stage" is not disclosed in the Specification. According to the Patent Rules § 1.71(a), The specification must include a written description of the invention or discovery and of the manner and process of making and using the same, and is required to be in such full, clear, concise, and exact terms as to enable any person skilled in the art or science to which the invention or discovery appertains, or with which it is most nearly connected, to make and use the same. Such omission would prevent one of ordinary skill in the art from making and using the invention.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chambers et al. (US 3,818,128) in view of Watanabe et al. (US 6,373,671) and Applicant Admitted Prior Art (AAPA). Chambers et al. disclose following elements of the claim including: a main deflection circuit for generating a main deflection current in a

Art Unit: 2836

main deflection winding to scan an electron beam on a screen of a cathode ray tube (31 in Fig. 2); a first amplifier stage for generating an auxiliary deflection current in an auxiliary deflection winding (23 in Fig. 2) to correct a raster distortion (27 in fig. 2); a power supply output transistor generating a first power supply current of a load circuit and a second power supply current of said first amplifier stage (239 and 240 in Fig. 4). However, it does not disclose a sensor and a switch for controlling the power supply of the first amplifier stage. Watanabe et al. disclose a single power source (2 in Fig. 1) feeding plural loads (10a – 10d in Fig. 1) and including a sensor (3a in Fig. 1) detecting an occurrence a fault condition in a current path of said power supply current of the first load (10a in Fig. 1) and a first power switch (9a in Fig. 1) responsive to an output of the sensor selectively reducing the second power supply current of the first load, without interrupting the power supply current of other load circuits, when the fault condition occurs (col. 5, line 54 – col. 6, line 65). In the Chambers et al. system modified according to Watanabe et al., the first power switch will selectively reduce (disconnect) the second power supply current of the first amplifier stage, without interrupting the power supply current of other load circuits. Both references have the same problem solving area, namely providing power supply a single power supply source to plural loads together with an overcurrent protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Chambers et al. solution by adding the current protection solution of Watanabe et al., because according to AAPA (page 1, lines 20 – 26), trouble shooting convenience requires that the TV receiver show a picture when the convergence circuit have a fault.

Thus, the rest of the TV receiver circuits including the deflection circuits remain energized and operational.

Regarding Claim 2, in the Chambers et al. system modified according to Watanabe et al., the first power switch (9a in Fig. 1 in Watanabe) decouples the first amplifier stage (27 in Fig. 2 in Chambers) from the power supply output transistor (239 and 240 in Fig. 4 in Chambers), when the fault condition occurs (col. 5, line 54 – col. 6, line 65 in Watanabe). A motivation for modification of the primary reference is the same as above.

Regarding Claim 4, Chambers et al. disclose load circuit as an output stage of the deflection circuit (31 in Fig. 2).

Regarding Claim 5, in the Chambers et al. system modified according to Watanabe et al., the output stage of the deflection circuit (31 in Fig. 2 in Chambers) continues operating and the first amplifier stage (27 in Fig. 2 in Chambers) ceases generating the auxiliary deflection current, when the fault condition occurs. A motivation for modification of the primary reference is the same as above.

Claims 6 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chambers et al. in view of Watanabe et al., AAPA and Rodriguez-Cavazos (US 4,961,032). As was stated above, Chambers et al., Watanabe et al. and AAPA disclose all the elements of Claim 1. Regarding Claim 6, Chambers et al. further disclose a transformer (105 in Fig. 4) coupled to the power supply output transistor (239 and 240 in Fig. 4) and generating a plurality of the power supplies shown in Fig. 7. However,

Art Unit: 2836

they do not disclose the second amplifier stage and the second switch. Rodriguez-Cavazos discloses the circuit generating the auxiliary deflection signal for CDT having the second amplifier (bottom part of the circuit in Fig. 3) for generating a second, negative, portion of the auxiliary deflection current, fed by at least two power supplies, positive and negative (+50, +15V and -50, -15V in Fig. 3). Both references have the same problem solving area, namely generating the auxiliary signal deflection signal for CRT. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Chambers et al. solution by adding the second amplifier according to Rodriguez-Cavazos, because as Rodriguez-Cavazos states (col. 2, lines 36 – 45), such type of class B amplifier significantly reduces the power dissipation in output convergence amplifiers by utilizing two different power supplies during distinctly different portions of the waveforms, that is, during trace and retrace. As to the second switch, Watanabe discloses plurality of the switches (9a – 9d in Fig. 1), one per each output. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Chambers et al. solution by adding the second switch responsive to the same control signal and disconnecting the second amplifier stage from the supply transformer, when the fault condition occurs, because disconnection of only one part of the Rodriguez-Cavazos amplifier would not resolve a problem of the short circuit in the auxiliary coil, since both amplifiers are connected to the coil.

Regarding Claim 3, Chambers et al. disclose the main deflection winding including both the vertical deflection winding (22 in Fig. 2) and horizontal (21 in Fig. 2)


Art Unit: 2836

and it further discloses the auxiliary winding (23 in Fig. 2). However, it does not explicitly state this winding being used for convergence purpose. Rodriguez-Cavazos discloses the circuit generating the deflection signals for auxiliary winding, i.e. convergence winding (col. 1, lines 4 – 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Chambers et al. solution by applying his circuit for generating the deflection signals for convergence coils, because as Chambers et al. state (col. 1, lines 10 – 30) such winding is necessary to correct distortions of the video image.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.  
08/26/2005



BRIAN SIRCUS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800